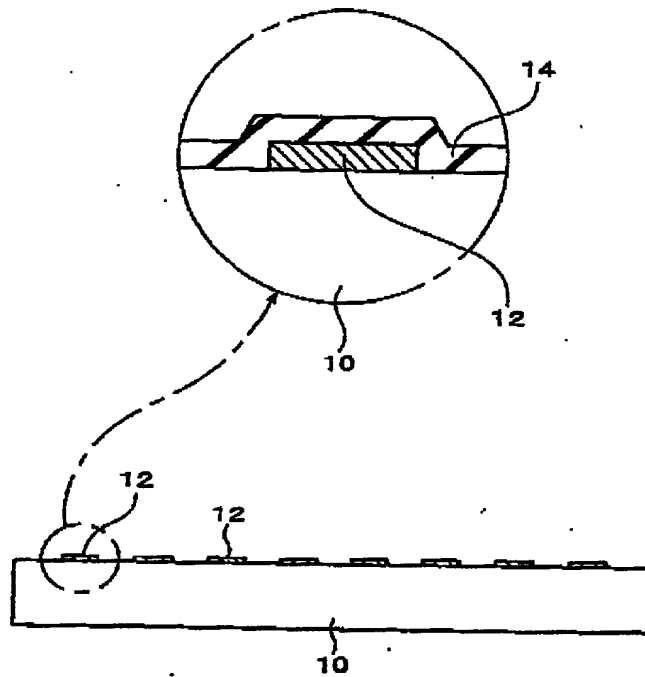


[NAME OF DOCUMENT]

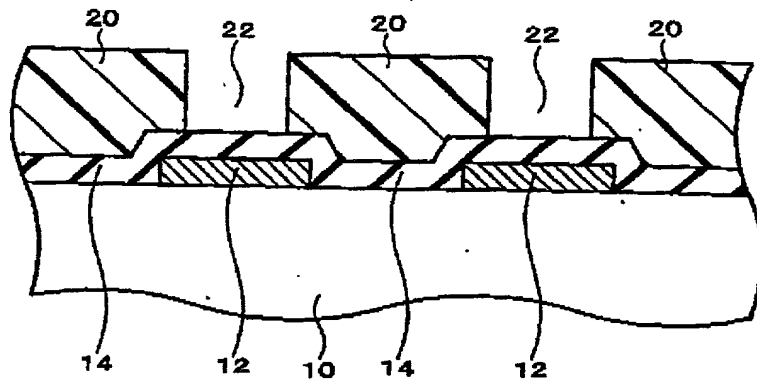
DRAWINGS

[FIG. 1]

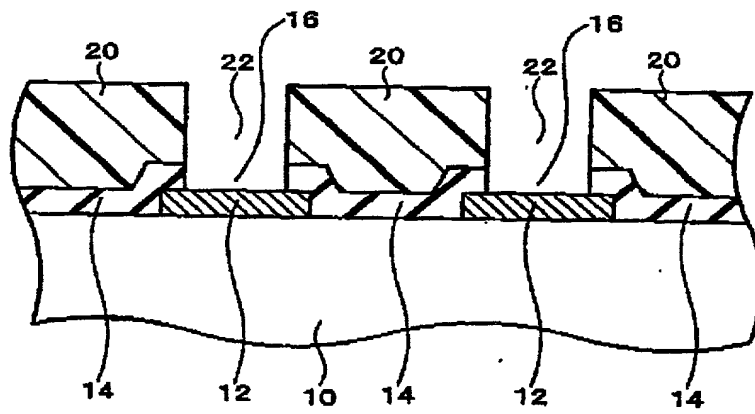


[FIG. 2]

(A)

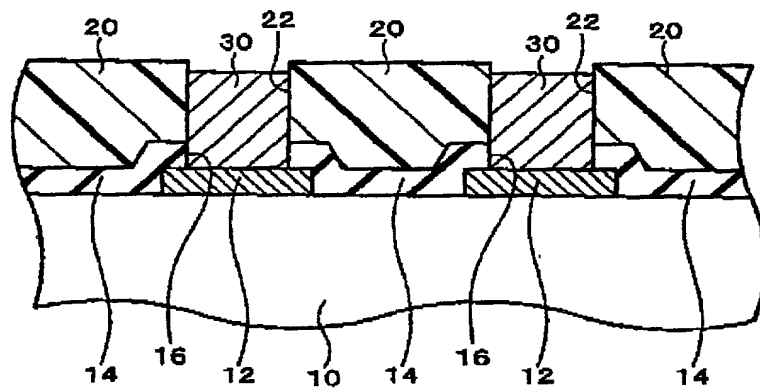


(B)

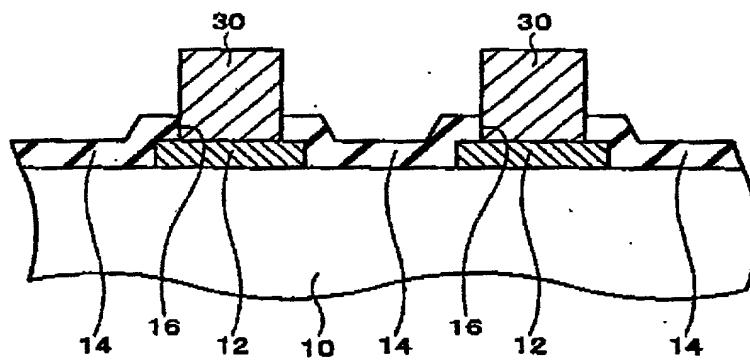


[FIG. 3]

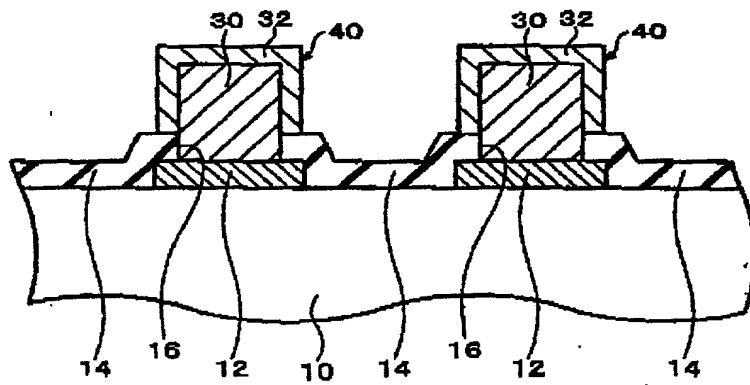
(A)



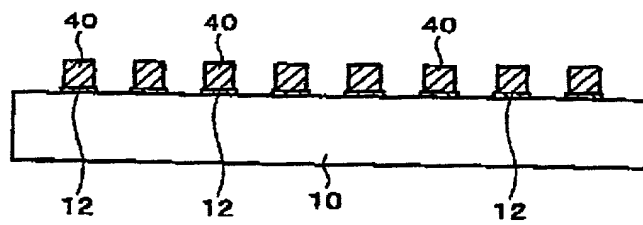
(B)



(C)

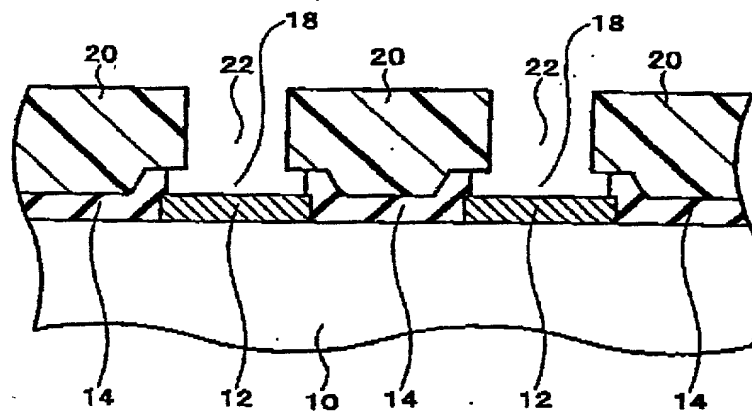


[FIG. 4]

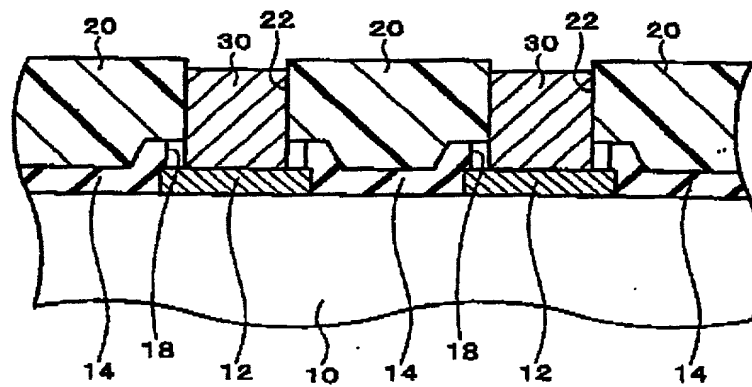


[FIG. 5]

(A)

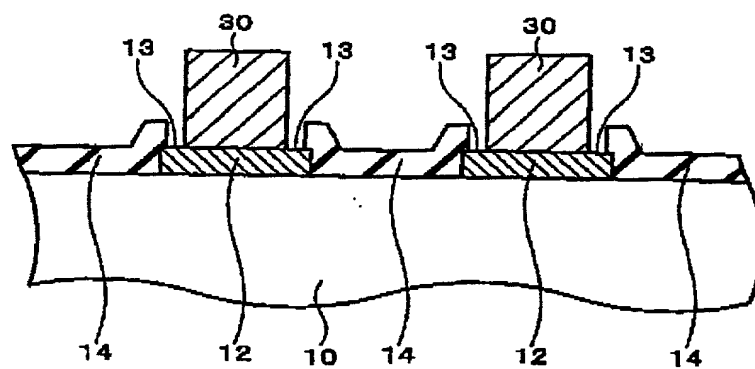


(B)

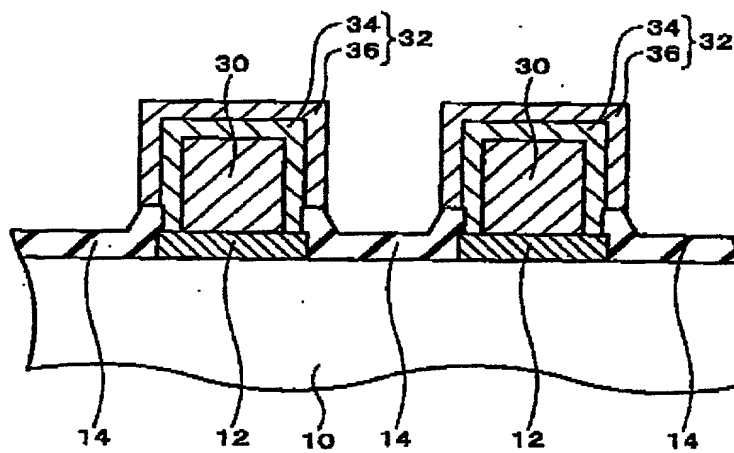


[FIG. 6]

(A)

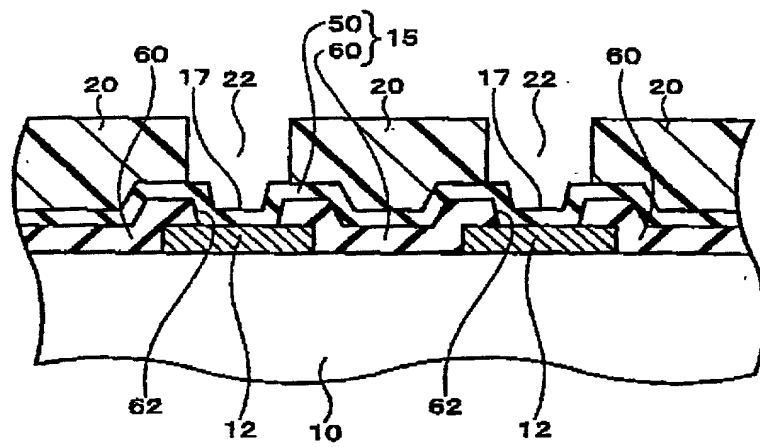


(B)

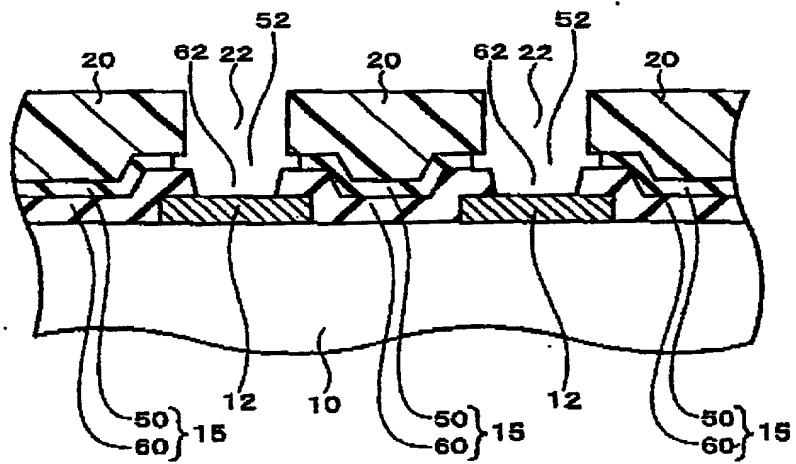


[FIG. 7]

(A)

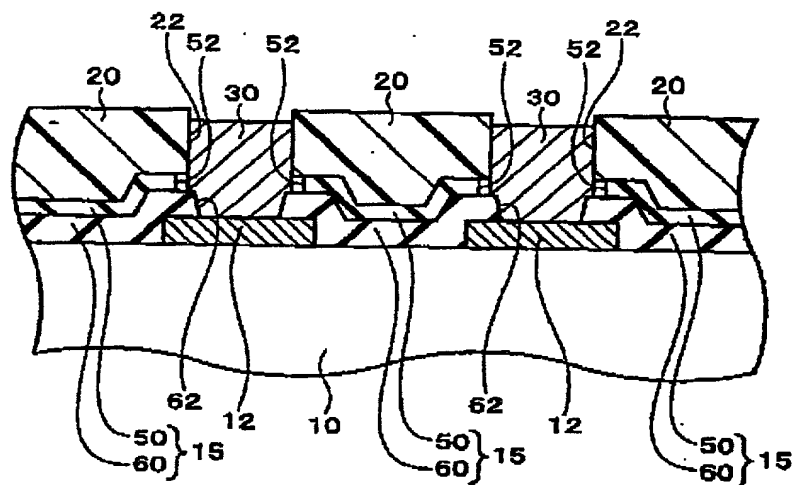


(B)

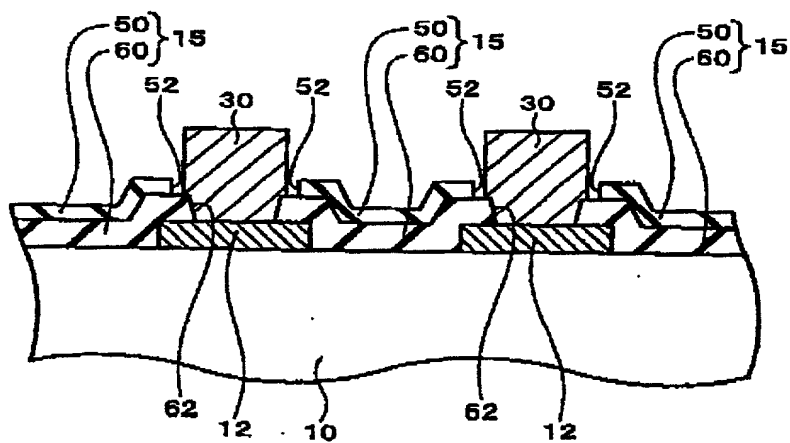


[FIG. 8]

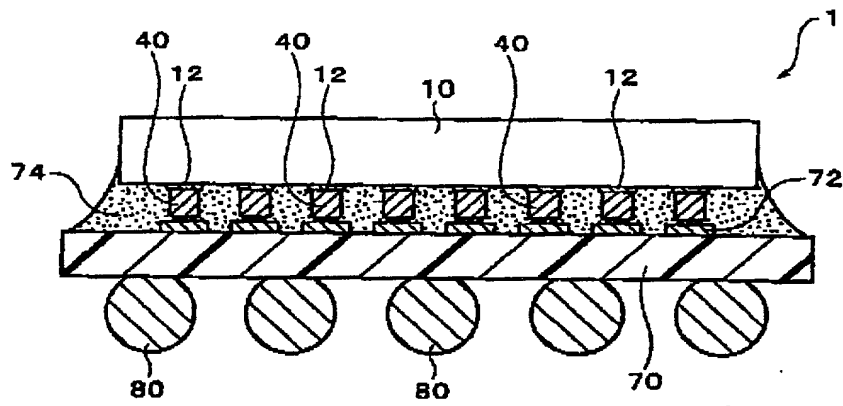
(A)



(B)



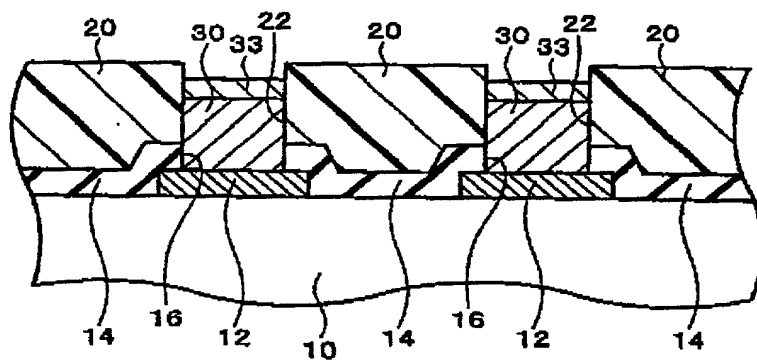
[FIG. 9]



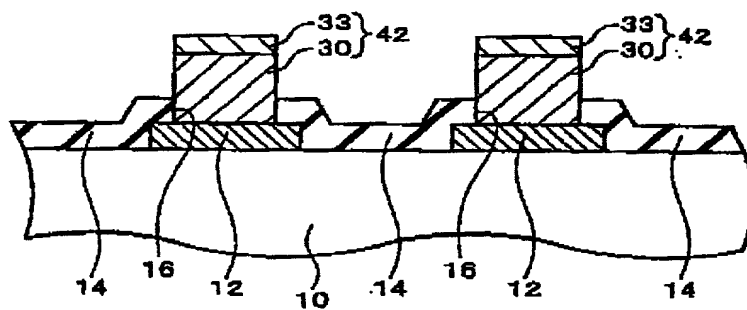


[FIG. 10]

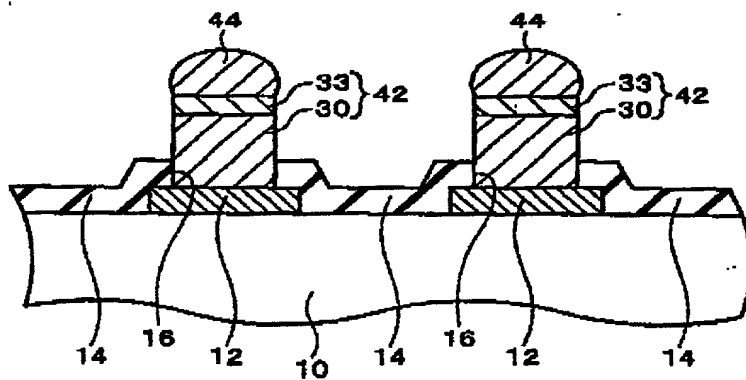
(A)



(B)

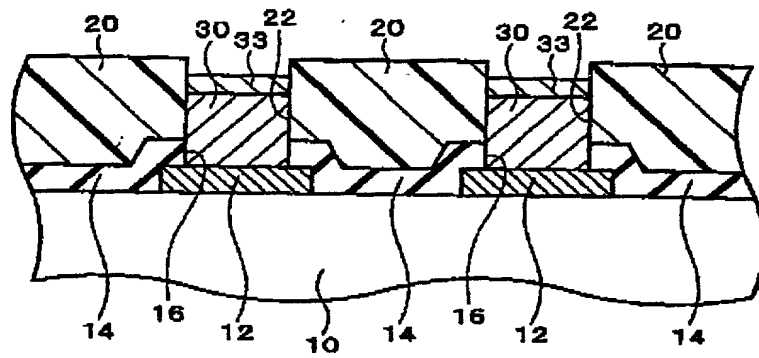


(C)

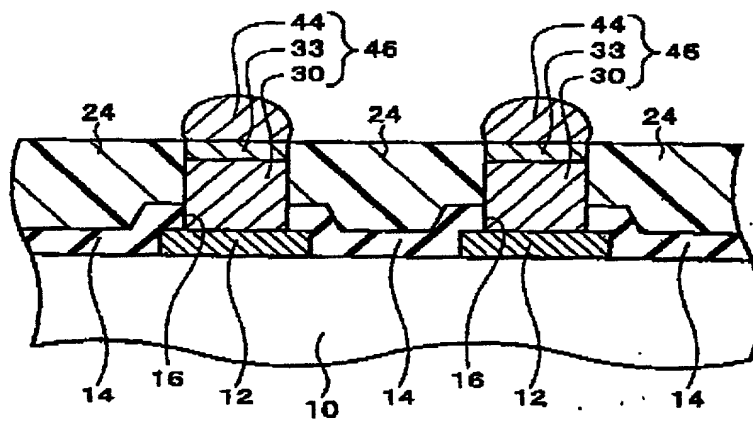


[FIG. 11]

(A)

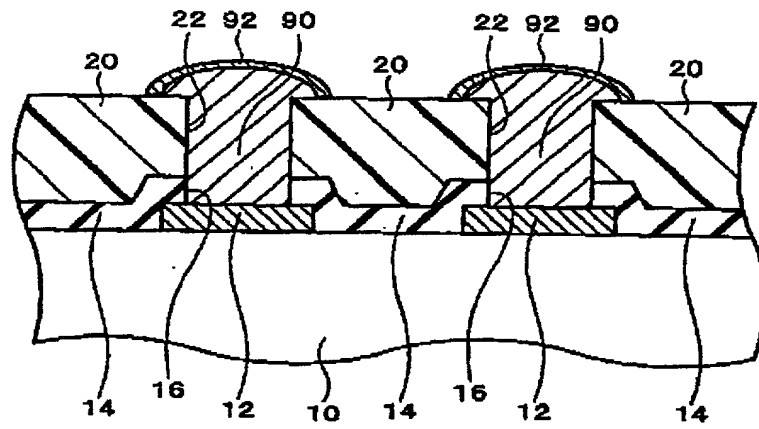


(B)

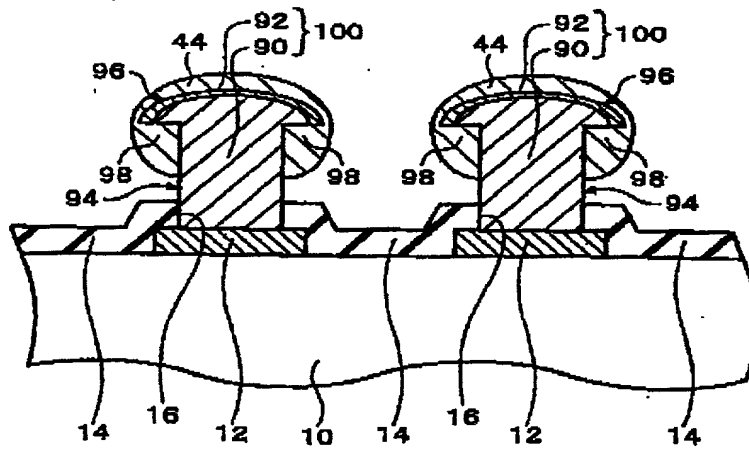


[FIG. 12]

(A)

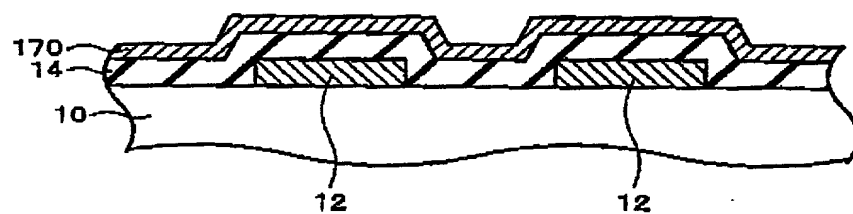


(B)

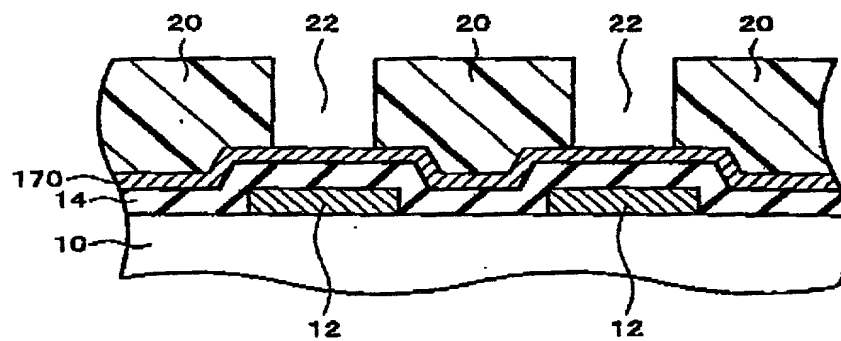


[FIG. 13]

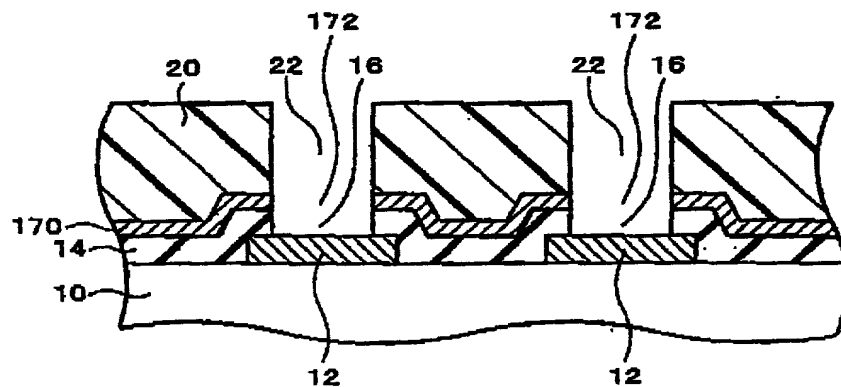
(A)



(B)



(C)

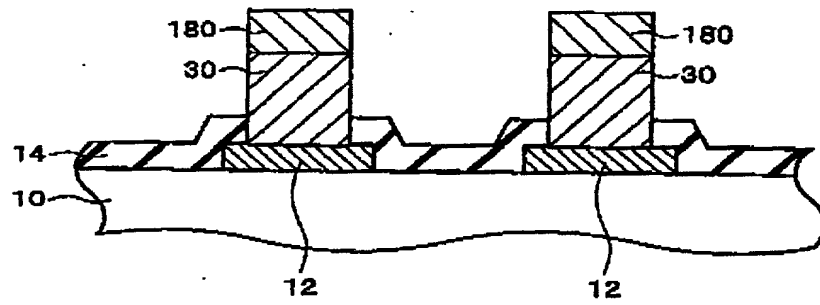


[illegible]

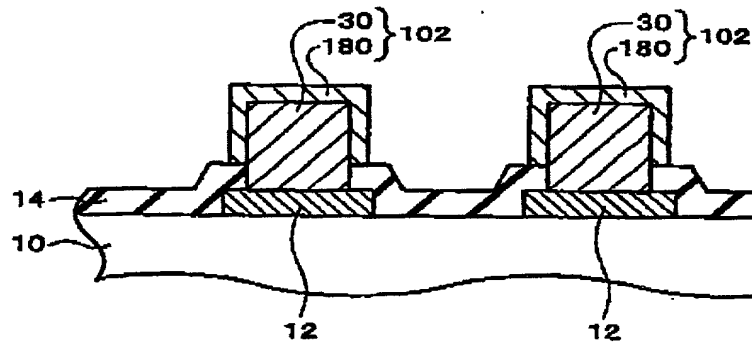
This cross-sectional view shows a substrate 10 with a patterned layer 12 on top. Two gate structures are formed on the substrate. Each gate structure consists of a gate stack 30 and a gate cap 180. The gate stack 30 is composed of a gate dielectric 14 and a gate conductive layer 170. The gate cap 180 is a conductive layer on top of the gate stack. The gate structures are separated by a trench 12.

[FIG. 15]

(A)

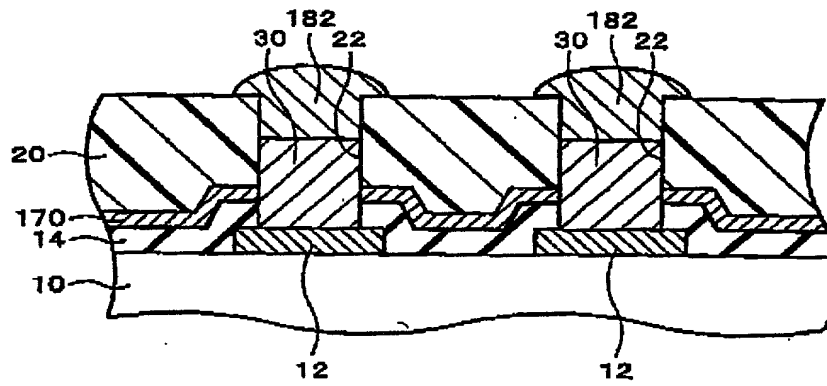


(B)

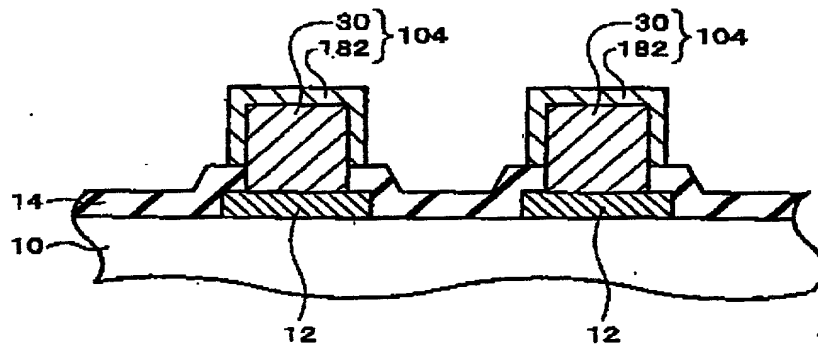


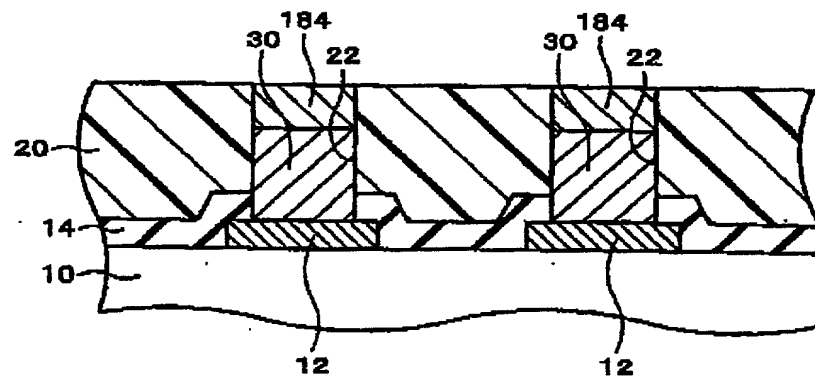
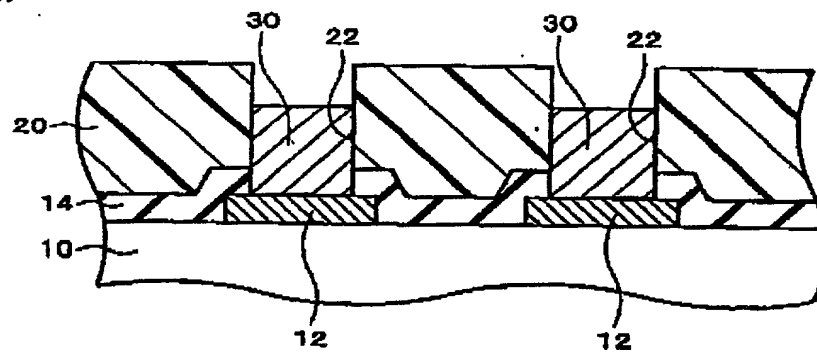
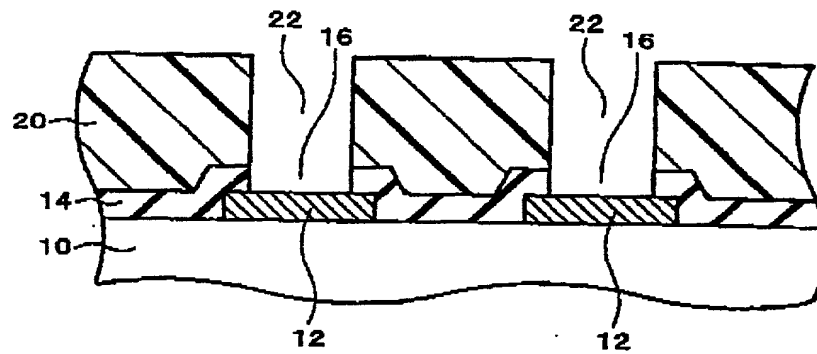
[FIG. 16]

(A)



(B)

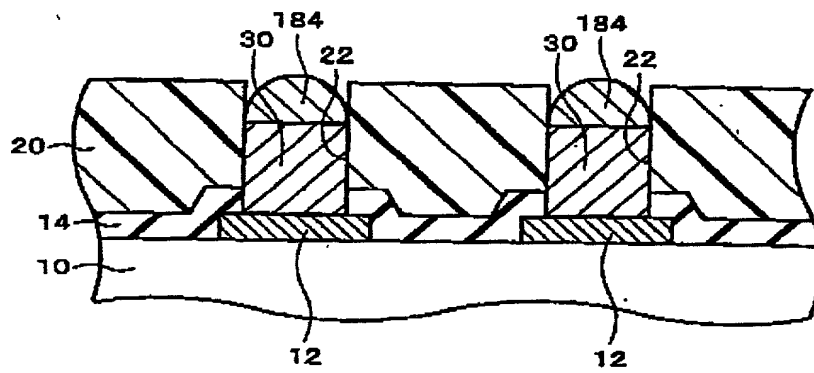


[illegible]

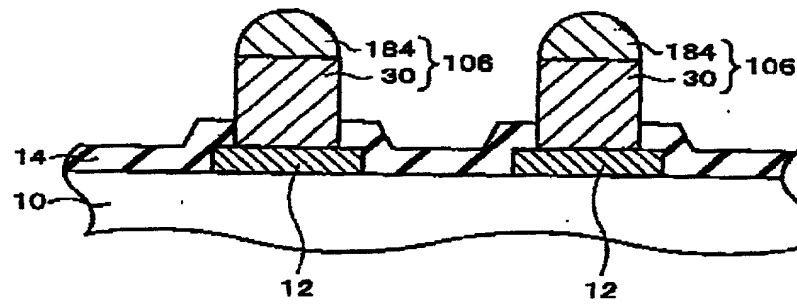


[FIG. 18]

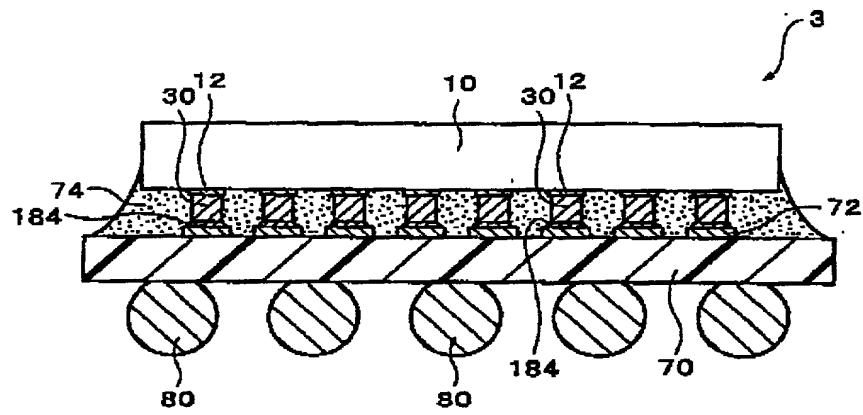
(A)



(B)

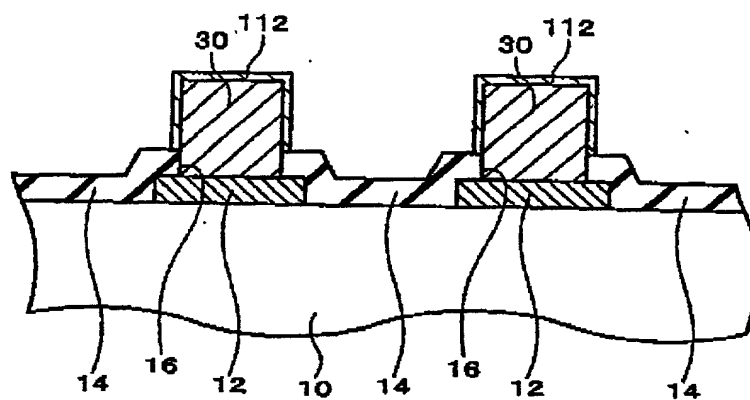


[FIG. 19]

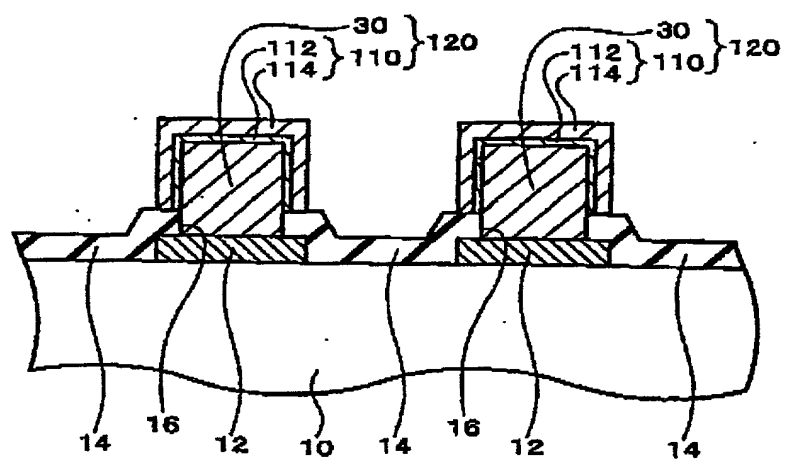


[FIG. 20]

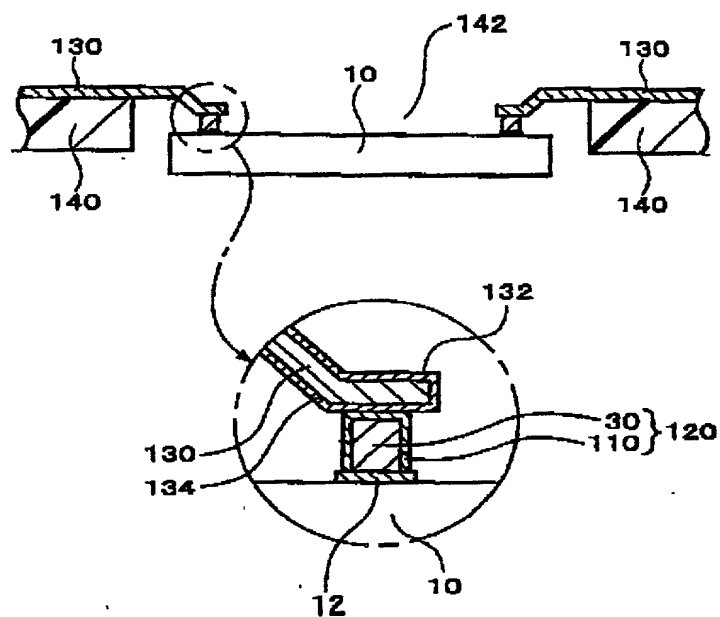
(A)



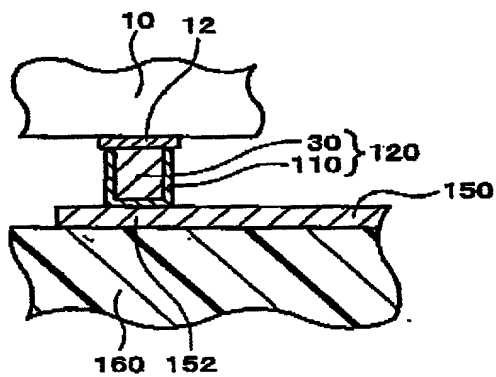
(B)



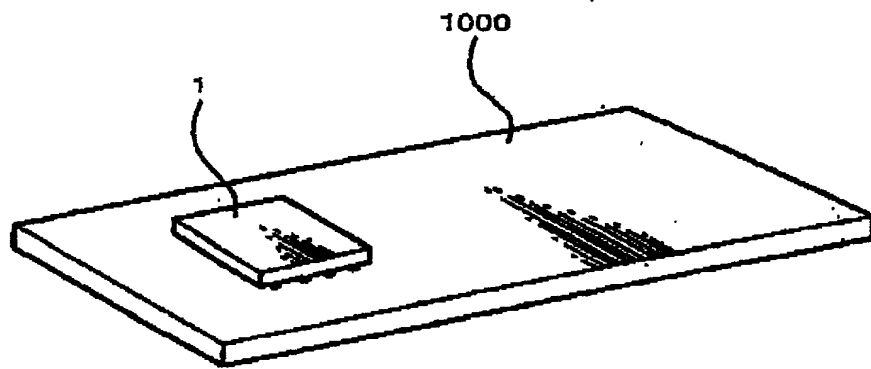
[FIG. 21]



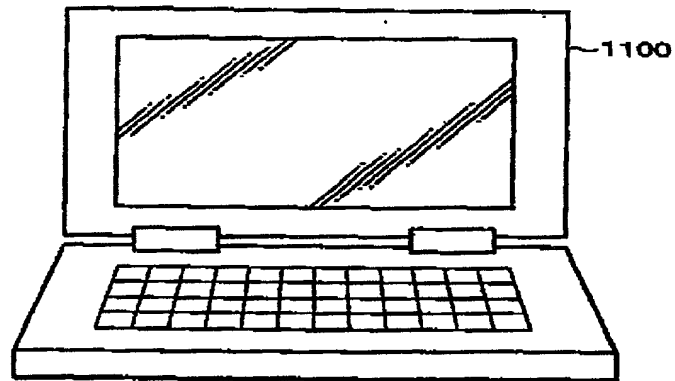
[FIG. 22]



[FIG. 23]



[FIG. 24]



[FIG. 25]

